In the Specification

Please disregard and/or reverse the amendments to the Specification made in the Amendment submitted by Applicant on July 5, 2005.

Please amend the three paragraphs [0025] through [0027] as follows:

[0025] Figure 7 illustrates a subsequent stage of processing in which the first and second spacer layers 450 and 600 are patterned by a vertical etch process 700 to form first and second spacers, which bear the same reference numbers, respectively. As a result of the vertical etch process, the first spacers 450 exhibit an "L" shape, each having a vertically oriented or "vertical" portion 460 extending in a direction generally parallel to the sidewall of the PC gate stack 110, and a horizontally oriented or "horizontal" portion 470 extending in a direction generally parallel to the surface of the active area 140. The horizontal portions 470 have edges 475 which are horizontally or laterally displaced from the walls 465 of the vertical portions 470 of the first spacers. As can be seen in Figure 7, the second spacers 600 extend along walls 465 of the vertical portions 460 so as to vertically overlie the horizontal portions 470. As a consequence of the vertical etch process, the second spacers extend to the edges 475 of the first spacers. Preferably, this patterning is performed by a reactive ion etch (RIE) which is not selective to the material of either spacer layer, i.e. not selective to nitride or to oxide. Alternatively, a two-step etch can be performed to first etch the overlying layer 600 selective to nitride, and then etching the first layer 450 selective to oxide. At the conclusion of this etching procedure, the tops of the PC gate stacks 110 become

exposed between the first spacers 450 on the sidewalls of the gates.

[0026] Figure 8 is a cross sectional depiction of a subsequent processing stage. As shown in Figure 8, the NFET area 102 is masked, as shown at 800, while source and drain ion implants are performed to the active area 140 of the PFET 104. Once the mask 800 is in place, the source and drain regions in the PFET area 104 are ion implanted with a p-type dopant such as boron. With the presence of the first spacers 450 and second spacers 600, the ion implantation into the active area 140 is aligned with the edges 475 of the first spacers, thus aligning the source and drain regions of the PFET to the edges 475 of the first spacers. The implants in the source and drain regions are depicted by reference number 860. After the completion of the source and drain ion implants for the PFET, the mask 800 is removed and post clean-up procedures are conducted following such removal.

[0027] After the source and drain regions are implanted in the PFET 104, processing proceeds to implanting source and drain regions in the NFET 102. As shown in Figure 9, the second ~~spacer~~ spacers 600 ~~is~~ are removed from the structures in areas 102 and 104, as by a blanket wet etch selective to silicon nitride. Such wet etch results in removal of the oxide layer 400 as well, where exposed in areas that do not underlie the first (nitride) ~~spacer~~ spacers 450. At the conclusion of this stage of processing, with the removal of the second spacers 600, the horizontal portions 470 of the first (nitride) spacers are exposed. ~~exhibit an "L" shape having a vertically oriented portion 460 extending in a direction generally parallel to the sidewall of the PC gate stack 110, and a horizontally oriented portion 470 extending in a direction generally parallel to the~~

~~surface of the active area 140.~~

Please amend paragraph [0029] as shown in the following:

[0029] The etching process removes the horizontally oriented portion 470 of the spacer in the NFET area 102 while leaving the vertically oriented portion 460 in place. After such etch, source and drain implants are performed to the NFET area 102 in the same direction as the direction of the prior anisotropic etch 1000, to produce source and drain regions 150 aligned to walls of the vertically oriented portions of the first spacers, the source and drain regions 150 thus being ~~which are~~ self-aligned to the channel region of the NFET 102. Such implantation is masked by the remaining portion of first spacer 450 and the PC gate 110. The spacing of the source and drain regions 150 are determined by the width of the remaining portion 460 of the spacer.